File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200432
(c) 2004 Thomson Derwent

Set	Items	Description
S1	554144	PULSE OR PULSES OR PULSETRAIN? OR WAVEFORM? OR WAVE()FORM? ?
S2	34883	S1(3N)(SERIES OR RANGE? ? OR INTERVAL? ? OR SEQUENCE? OR SUBSEQUENCE? OR STRING? ? OR SUBSTRING? OR SUCCESSION? OR CONTINUUM? OR ROW? ?)
S3	544566	FIELD? ? OR SUBFIELD? OR FIELDNAME?
S4	10626	S1(3N)(POSITION? OR LOCATION? OR PLACE? ? OR PLACEMENT? OR PLACE()MENT? ?)
S5	2493	S1(10N)(TABLE? OR DATABASE? OR DATASET? OR DATABANK? OR DB OR DATAFILE? OR DIRECTORY? OR DIRECTORIES)
S6	733	S1(10N)(DATADICTIONAR? OR DATA()(FILE? ? OR BASE? ? OR BANK? ? OR DICTIONAR? OR SET? ?))
S7	424	UWB OR (ULTRAWIDE OR ULTRA()WIDE OR UW OR U()W)()(BAND OR BANDWIDTH) OR ULTRA()WIDEBAND
S8	15426	S1(3N)(ENCOD???? ? OR INCOD???? ? OR COD???? ? OR SUBCOD???? ? OR MICROCOD???? ? OR CODIFY? OR CODIFIE? ? OR CODIFIC?)
S9	1322	S8(3N)(SENT OR SEND??? ? OR TRANSMIT? OR TRANSMIS? OR COTRANSMIT? OR COTRANSMIS? OR TRANSFER? OR XFER? OR DISBURS? OR STREAM? OR DISPERS?)
S10	490	S8(3N)(DISTRIBUT? OR COMMUNICAT? OR RELAY? OR TELECOMMUNICAT? OR CYBERCAST? OR NETCAST? OR BROADCAST? OR MULTICAST? OR WEBCAST?)
S11	1	S8(3N)(CYBER OR NET OR BROAD OR MULTI OR WEB)()CAST???? ?
S12	36	S8(3N)(EXCHANG? OR DISSEMINAT?)
S13	973	S2 AND S4
S14	12	S13 AND S5:S6
S15	153	S4 AND S5:S6
S16	1	S15 AND (S7 OR S9:S12)
S17	2506	S2 AND S3
S18	24	S17 AND S5:S6
S19	122	S5:S6 AND S3
S20	1	S19 AND (S7 OR S9:S12)
S21	38	S14 OR S16 OR S18 OR S20
S22	38	IDPAT (sorted in duplicate/non-duplicate order)
S23	38	IDPAT (primary/non-duplicate records only)

23/9/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014511130 **Image available**
WPI Acc No: 2002-331833/200237
XRPX Acc No: N02-260555
Pulse position **determination apparatus for signals** encoded **by** pulse **modulation in wireless** communication , **has probability** table **providing value representing** pulse position , **based on reception of channel signals**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC); GFELLER F (GFEL-I); HIRT W (HIRT-I)
Inventor: GFELLER F; HIRT W
Number of Countries: 030 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1172978	A2	20020116	EP 2001111206	A	20010514	200237	B
CN 1332533	A	20020123	CN 2001122453	A	20010709	200237	

JP 2002141873 A 20020517 JP 2001207719 A 20010709 200237
US 20020017949 A1 20020214 US 2001902365 A 20010710 200237
KR 2002005961 A 20020118 KR 200138293 A 20010629 200250

Priority Applications (No Type Date): EP 2000810601 A 20000710
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 1172978 A2 E 24 H04L-025/49
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
CN 1332533 A H04B-014/02
JP 2002141873 A 23 H04B-014/02
US 20020017949 A1 H03K-009/04
KR 2002005961 A H04B-014/04

Abstract (Basic): EP 1172978 A2

NOVELTY - A memory (118) such as ROM or RAM stores a probability table (110) which provides a set of values (DDS) (C1-C4) representing the **pulse position** , in response to receipt of a primary channel signal (PCS) and a diversity channel signal (DCS). The probability table is a diagonally asymmetric table or symmetric table which is based on Bayes' probability.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) **Pulse position** determination method;
(b) Digital signal reception method;
(c) Digital signal receiver system;
(d) Computer program for **pulse position** determination

USE - For determining **pulse position** for signal **encoded** by **pulse** modulation in wireless **communication** system.

ADVANTAGE - The **pulse position** of the signal, is determined accurately, without signal quality consideration. Avoids need for complex modulation techniques.

DESCRIPTION OF DRAWING(S) - The figure shows the dual-channel symbol detector. (Drawing includes non-English language text).

Probability table (110)
Memory (118)
Pulse position representing values (C1-C4)
pp; 24 DwgNo 16/22

Title Terms: PULSE; POSITION; DETERMINE; APPARATUS; SIGNAL; ENCODE; PULSE; MODULATE; WIRELESS; COMMUNICATE; PROBABILITY; TABLE; VALUE; REPRESENT; PULSE; POSITION; BASED; RECEPTION; CHANNEL; SIGNAL
Derwent Class: W01
International Patent Class (Main): H03K-009/04; H04B-014/02; H04B-014/04; H04L-025/49
International Patent Class (Additional): H04B-010/00; H04B-010/02; H04B-010/10
File Segment: EPI
Manual Codes (EPI/S-X): W01-A02; W01-A08A1A

23/9/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011840682 **Image available**
WPI Acc No: 1998-257592/199823
XRPX Acc No: N98-203886
Wireless optical synchronizing circuit for PPM communication system e.g. wireless LAN - has controller which carries out synchronous control of

frame data based on output of detector
Patent Assignee: RICOH KK (RICO)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10084337	A	19980331	JP 96260277	A	19960909	199823	B

Priority Applications (No Type Date): JP 96260277 A 19960909
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10084337	A		6	H04L-007/00	

Abstract (Basic): JP 10084337 A

The circuit has a receiver which receives the transmitted **pulse position** modulation signal. The received modulation signal is demodulated. A measurement unit measures the **pulse interval** of the received signal.

A detector detects the time required for obtaining **pulse** of maximum **interval** . A controller performs synchronous control of frame **data based** on detection signal of detector.

ADVANTAGE - Performs high speed data electrical transmission. Shortens regeneration time. Simplifies structure. Facilitates radio transmission. Reduces signal error.

Dwg.1/5

Title Terms: WIRELESS; OPTICAL; CIRCUIT; COMMUNICATE; SYSTEM; WIRELESS; LAN ; CONTROL; CARRY; SYNCHRONOUS; CONTROL; FRAME; DATA; BASED; OUTPUT; DETECT
Derwent Class: W01
International Patent Class (Main): H04L-007/00
International Patent Class (Additional): H04J-013/00; H04L-025/49
File Segment: EPI
Manual Codes (EPI/S-X): W01-A04A; W01-A06B5A; W01-A06C3; W01-A08A1A

23/9/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009373148 **Image available**
WPI Acc No: 1993-066627/199308
XRPX Acc No: N93-050991
Digital video pulse **width and** position **modulator - includes RAM look-up** tables **for translating series of data words into** series **of** pulse **attribute words**
Patent Assignee: XEROX CORP (XERO)
Inventor: CIANCIOSI M S
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5184226	A	19930202	US 91783011	A	19911025	199308	B
JP 5259838	A	19931008	JP 92279782	A	19921019	199345	
JP 3399565	B2	20030421	JP 92279782	A	19921019	200328	

Priority Applications (No Type Date): US 91783011 A 19911025
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5184226	A		19	H04N-001/40	
JP 5259838	A			H03K-005/04	
JP 3399565	B2		14	H03K-005/04	Previous Publ. patent JP 5259838

Abstract (Basic): US 5184226 A

The digital electronics system generates **pulses** from a **series** of data words and includes RAM look-up tables for translating the series of data words into a **series** of **pulse** attribute words. Each pulse attribute word includes information for controlling the formation of a corresponding pulse, multiplexers for splitting the **series** of **pulse** attribute words into two channels and pulse forming circuits corresponding to each channel for accepting pulse attribute words from respective channels and forming pulses using the information included in the pulse attribute words.

Control circuits generates the pulses, where a pulse from a first pulse forming circuit is generated while a pulse from a second pulse forming circuit is being formed.

ADVANTAGE - Can process video signal into video pulses at high speed without use of expensive, high speed pulse forming circuits.

Dwg.12/12

Title Terms: DIGITAL; VIDEO; PULSE; WIDTH; POSITION; MODULATE; RAM; LOOK-UP ; TABLE; TRANSLATION; SERIES; DATA; WORD; SERIES; PULSE; ATTRIBUTE; WORD
Derwent Class: P75; T04; W02
International Patent Class (Main): H03K-005/04; H04N-001/40
International Patent Class (Additional): B41J-002/44; G01D-009/42; H04N-001/04
File Segment: EPI; EngPI
Manual Codes (EPI/S-X): T04-G04; T04-G10A; W02-J02B2B; W02-J03A3
? t23/9/27,31,33,35

23/9/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004750277
WPI Acc No: 1986-253618/198639
XRPX Acc No: N86-189662

Function generator for NMR system - has synthesiser modules producing analog waveforms and program controller generating information and general fields

Patent Assignee: ADV NMR SYST INC (ADNM-N)
Inventor: BRIGGS R L
Number of Countries: 012 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 195670	A	19860924	EP 86302040	A	19860319	198639	B
US 4707797	A	19871117	US 85713785	A	19850320	198748	
EP 195670	B	19890809				198932	
DE 3664964	G	19890914				198938	

Priority Applications (No Type Date): US 85713785 A 19850320
Cited Patents: 1.Jnl.Ref; A3...8722; No-SR.Pub; US 4318043
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 195670	A	E	23		
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
EP 195670	B	E			
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					

Abstract (Basic): EP 195670 A

The synthesizer has a memory and an address sequencer for producing a sequence of addresses for the memory. Data is entered into the memory from an external source. Portions of data are sequentially retrieved in accordance with the address sequences. The retrieved data includes an

instruction field for controlling the operation of the **sequencer** , an analog **waveform field** and a digital waveform **field** .

An analog synthesizer responds to the analog waveform **field** to produce the analog output. A subroutine generates the analog waveform **field** as a concatenation of elementary waveform segments and a program controller controls the sequence of subroutine.

ADVANTAGE - Allows easy refurbishment, updating and maintenance

Abstract (Equivalent): EP 195670 B

A waveform synthesizer for an NMR imaging system, the synthesizer comprising a control system (70,72,74,242,168, 170,200,194) for generating an analog waveform output characterized in that the control system comprises a memory (70); an address sequencer (72) for producing a sequence of dynamically modifiable addresses (76) for the memory first means (242) for entering data into the memory from a source (26) external to the synthesizer, second means (74) for sequentially retrieving portions of the data from the memory in accordance with the sequence of addresses, the data retrieved from the memory including an instruction **field** for controlling the operation of the address **sequencer** , an 0analog **waveform field** for defining at least one analog waveform output and a digital output **field** for producing a plurality of digital outputs, analog waveform synthesizing means (168,170) responsive to the analog waveform **field** , for producing the air or each analog waveform output, and program means for generating the analog **waveform field** the program means including **data file** means (200) for defining a set of elementary **waveform** segments, subroutine means (194) for generating the analog waveform **field** as a concatenation of at least two of the elementary waveform segments and program control means for controlling the sequence of access to the data file means and the subroutine means. (29pp)

Abstract (Equivalent): US 4707797 A

The function generator includes several waveform synthesiser modules which are interconnected by a main bus to a central controller CPU. Each synthesiser is adapted to produce one analog waveform for the NMR imaging system. A synthesiser module includes a memory and an address sequencer which produces a sequence of addresses which control the retrieval of data from the memory. Each data world of the memory contains several **fields** . An instruction **field** and a general data **field** control the address sequencer so that the sequence of addresses is, in turn, controlled by the memory data. Other **fields** from the memory define analog and digital outputs produced by the synthesiser module.

The **fields** are generated by the program controller which is organised to have data segments which define a set of elementary analog waveform segments and subroutines which are controlled by a main program. The execution of each subroutine produces a segment of an analog waveform. The subroutines generate a segment by accessing given data segments and concatenating several elementary segments into a single analog output. Several synthesiser modules are interconnected by an interchannel communications bus which allows each synthesiser to signal every other synthesiser whereby the operations of the synthesisers can be synchronised. (23pp)e

Title Terms: FUNCTION; GENERATOR; NMR; SYSTEM; SYNTHESISER; MODULE; PRODUCE ; ANALOGUE; WAVEFORM; PROGRAM; CONTROL; GENERATE; INFORMATION; GENERAL; **FIELD**

Index Terms/Additional Words: NUCLEAR; MAGNETIC; RESONANCE

Derwent Class: S03; S05; T01

International Patent Class (Additional): G01N-024/08; G06F-015/31; G06J-001/00

File Segment: EPI

Manual Codes (EPI/S-X): S03-E07; S05-D02X; T01-J06A

23/9/31 (Item 31 from file: 347)
DIALOG(R)File 347:JAPIO
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06261318 **Image available**
DEVICE AND SYSTEM FOR SPEECH ENCODING AND DECODING

PUB. NO.: 11-202898 [JP 11202898 A]
PUBLISHED: July 30, 1999 (19990730)
INVENTOR(s): SERIZAWA MASAHIRO
APPLICANT(s): NEC CORP
APPL. NO.: 10-005224 [JP 985224]
FILED: January 14, 1998 (19980114)
INTL CLASS: G10L-009/14; G10L-009/18

ABSTRACT

PROBLEM TO BE SOLVED: To improve the encoding efficiency of the speech encoding and decoding device which can set an arbitrary encoding rate with a specified parameter by removing the generation of an ineffective encoding level regarding a multi- pulse signal.

SOLUTION: Subframe length is inputted to an input terminal 24A and passed to a subframe dividing circuit 10 and a unit length calculating circuit 32A. Basic vector length is inputted to an input terminal 26A and passed to the unit length calculating circuit 32A and a table designing circuit 34A. The unit length calculating circuit 32A calculates unit length determining **intervals** of **pulses** from the subframe length passed from the input terminal 24A and the basic vector length passed from the input terminal 26A and passes the unit length to a **table** converting circuit 30A. The **table** designing circuit 34A designs a **pulse position table** according to the number of **pulses** passed from an input terminal 28A and the basic vector length passed from the input terminal 26A and passes the table to the table circuit 36A.

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23/9/33 (Item 33 from file: 347)
DIALOG(R)File 347:JAPIO
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05258344 **Image available**
OPTIONAL WAVEFORM GENERATING DEVICE

PUB. NO.: 08-213844 [JP 8213844 A]
PUBLISHED: August 20, 1996 (19960820)
INVENTOR(s): ARAI MINORU
APPLICANT(s): SONY TEKTRONIX CORP [417165] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-034490 [JP 9534490]
FILED: January 31, 1995 (19950131)
INTL CLASS: [6] H03B-028/00
JAPIO CLASS: 42.4 (ELECTRONICS -- Basic Circuits)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

ABSTRACT

PURPOSE: To quickly generate an output signal obtained by replacing an optional part of an output waveform signal with an optional partial

waveform by providing a partial replacement memory and providing an output of partial replacement **waveform** data in place of basic **waveform** data within the **range** of designated addresses.

CONSTITUTION: The operator designates the desired **position** of a noise **waveform** to be overlapped on a sine wave signal waveform and the noise waveform itself while observing the waveform of a sine wave signal displayed on a display device 22 by an operation panel 16. Replacement waveform data such as the designated noise waveform or the like are stored in a partial replacement waveform memory 25. A microcomputer 10 sets an address range of sine wave signal **waveform** data of replacement **waveform** **data** **based** on the desired **position** and the replacement **waveform** data designated by the operator. Then waveform data of the sine wave signal being basic data are sequentially read from a waveform memory 18 and fed to a DAC 24 via a waveform data control circuit 23 and an output signal is generated via an LPF 26 and an output terminal 28. When the read address from the memory 18 reaches the start address of the replacement waveform data, noise waveform data are read from a memory 25 and fed to the DAC 24.

23/9/35 (Item 35 from file: 347)
DIALOG(R)File 347:JAPIO
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03772004 **Image available**
EXTRALOW-SPEED DRIVING DEVICE FOR PRECISE POSITIONING TABLE

PUB. NO.: 04-137104 [JP 4137104 A]
PUBLISHED: May 12, 1992 (19920512)
INVENTOR(s): SATO HIROSHI
SHIGETOMI HIDEMI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
SHOWA ELECTRIC WIRE & CABLE CO LTD [000225] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-259737 [JP 90259737]
FILED: September 28, 1990 (19900928)
INTL CLASS: [5] G05B-019/19
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation)
JAPIO KEYWORD:R002 (LASERS); R094 (ELECTRIC POWER -- Linear Motors)
JOURNAL: Section: P, Section No. 1411, Vol. 16, No. 407, Pg. 123, August 27, 1992 (19920827)

ABSTRACT

PURPOSE: To obtain a high precision by providing a target **pulse** generating means, a servo mechanism, and a table and generating second and following target **pulses** at prescribed **intervals** after generation of a first target pulse outputted from the target pulse generating means.

CONSTITUTION: A target **pulse** sending **interval** designating circuit 8 consists of a target pulse CPU 9, a target pulse storage circuit 10, and a target pulse designating interface 14, and a target value and position information are inputted through cable receivers 12 and 12 connected to terminals 8a and 8b and a data bus 11. An **interval** designating **pulse** P(sub 0) which designates the **intervals** of **position** target **pulses** P sent from a target pulse generating means 2 is sent to the means 2 through a cable driver 13, the interface 14, and a terminal 8c. The circuit 10 is provided with a target pulse designating program INDEXC and a register memory REG. The program INDEXC uses the memory REG to execute the sequence. When the program INDEXC is executed, the number of **position** target

pulses P and a number I of interpolations in a target section are stored in a **position** target **pulse** number register PR and an interpolation number register IR respectively by an initializing subroutine F(sub 1), and numerical values in a present section register iR and a zero return register KR are set to zero.
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